

FIG. 1

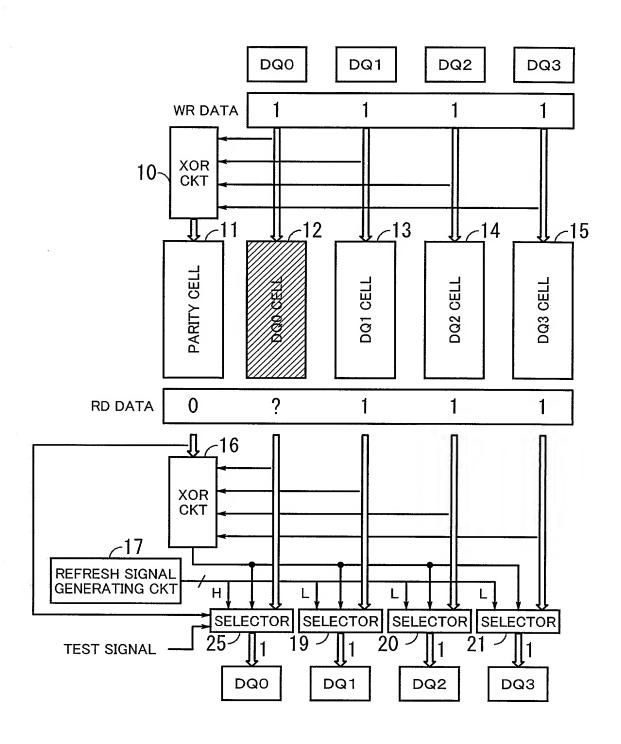
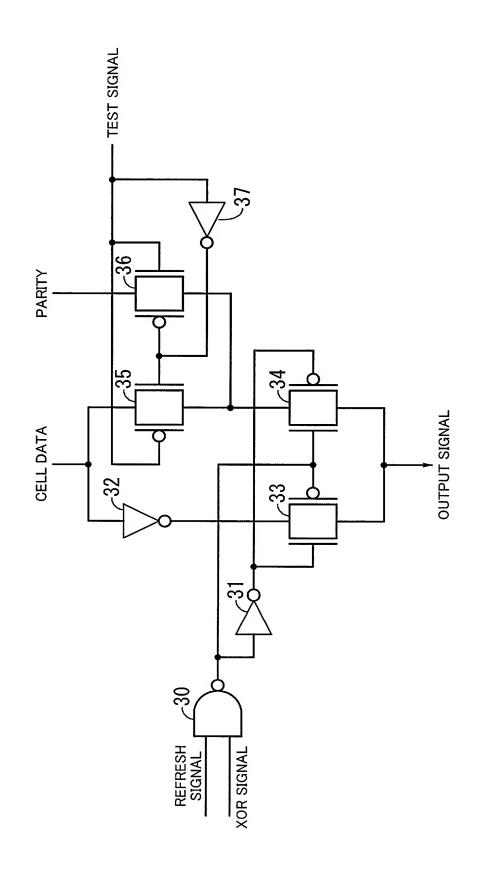


FIG. 2



F16. 3

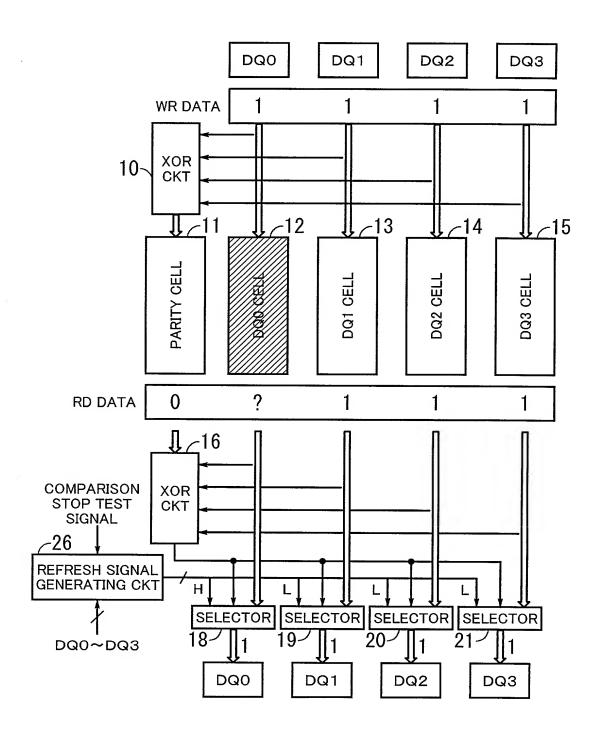


FIG. 4

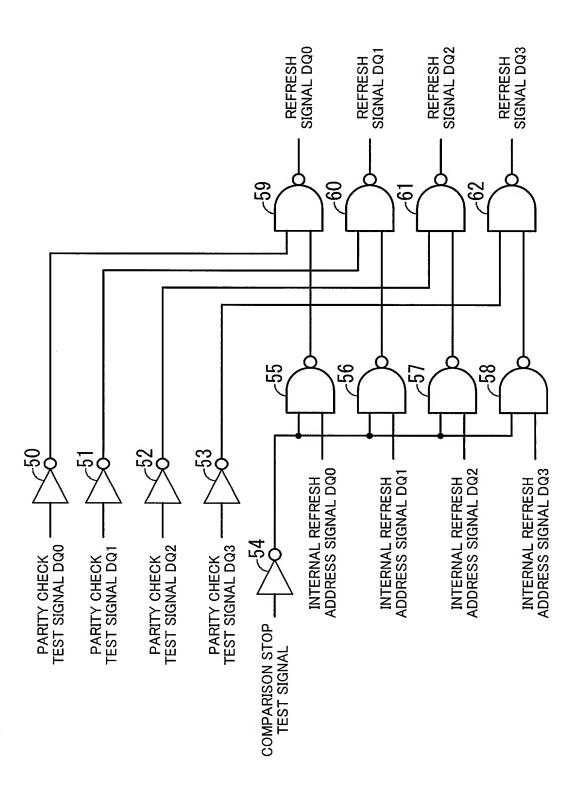


FIG. 5

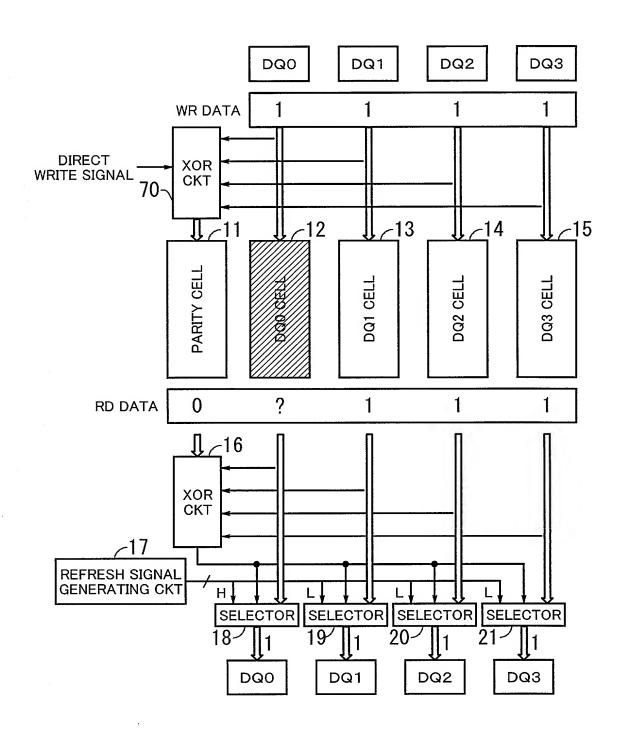


FIG. 6

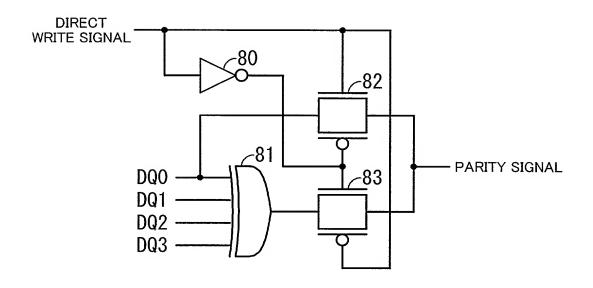


FIG. 7

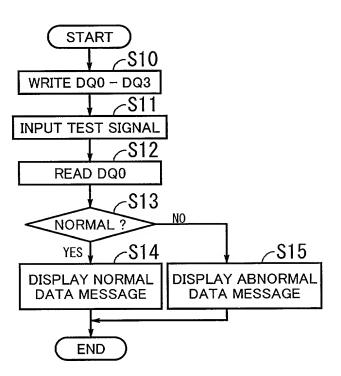


FIG. 8

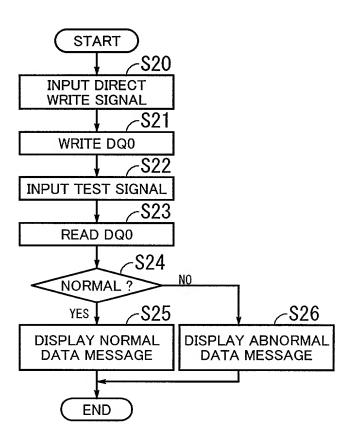


FIG. 9

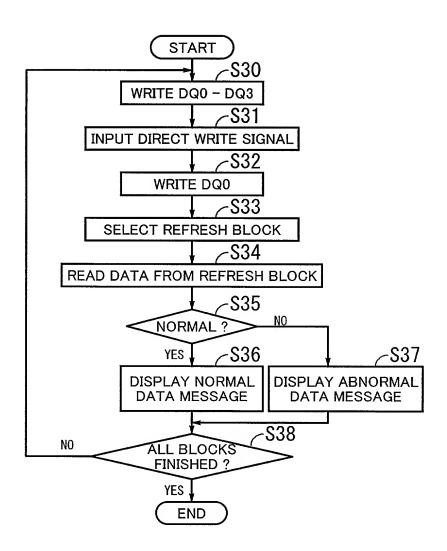


FIG. 10

MEMORY ARRAY PARITY ARRAY								
1-1	1-2	1-3	1-4	1P				
2-1	2-2	2-3	2-4	2P				
3-1	3-2	3-3	3-4	3P				
4-1	4-2	4-3	4-4	4P				

FIG. 11

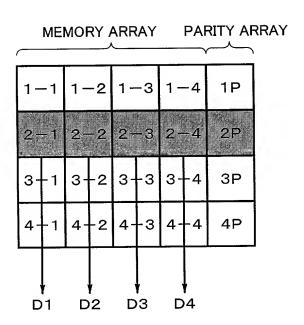


FIG. 12

MEMORY ARRAY PARITY ARRAY								
1-1	1-2	1-3	3	1-4	1P			
2-1	2-2		3	2-4	2P			
3-1	3-2	3-	3	3-4	3P			
4-1	4-2	4-	B	4-4	4P			
REFRESH BLOCK								

FIG. 13

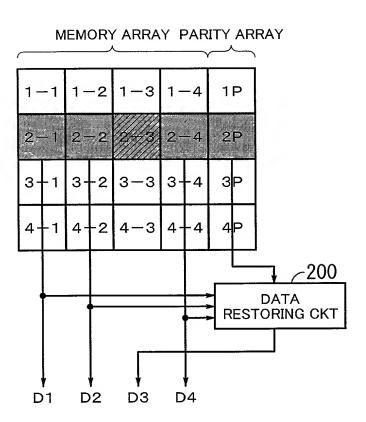


FIG. 14

. . . .

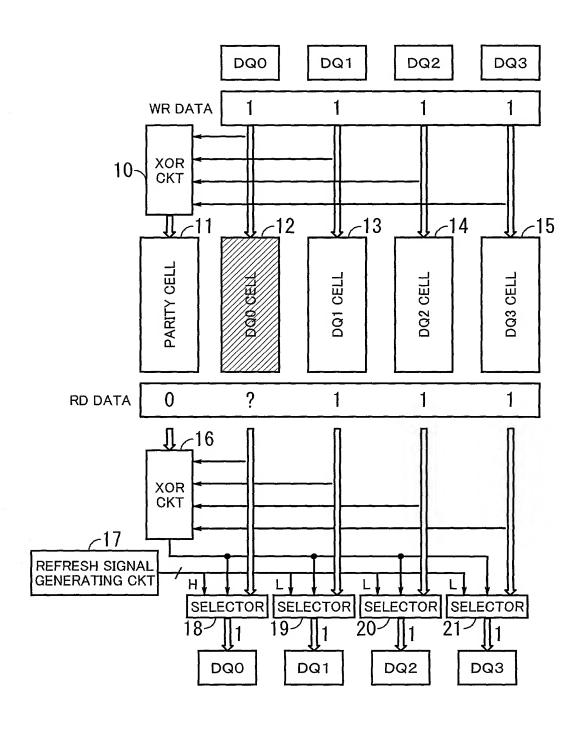


FIG. 15

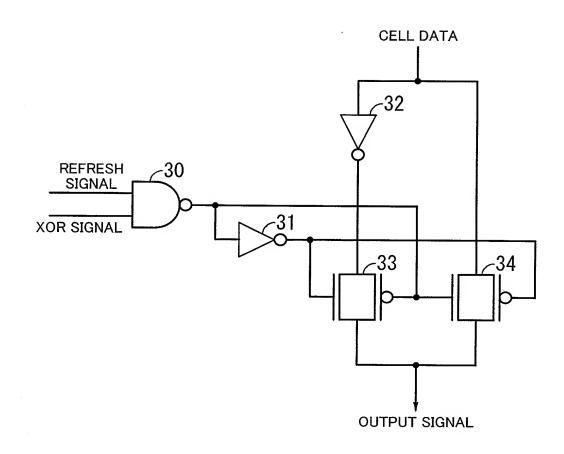


FIG. 16